This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

46. (Currently amended) An integrated circuit substrate comprising at least one buried conductor pattern provided within a monocrystalline substrate ~~and surrounded by semiconductor material~~ such that at least a portion of a top surface of said buried conductor pattern is below a top surface of said substrate and at least a portion of a bottom surface of said buried conductor pattern is above a bottom surface of said substrate, said at least one buried conductor pattern having a spherical pattern and forming at least a part of an interconnect between devices, and a conductive path extending from said buried conductor pattern to said devices.

47. (Previously amended) The integrated circuit of claim 46, further comprising a second buried conductor pattern having a pipe-shaped pattern.

48. (Previously amended) The integrated circuit of claim 46, further comprising a second buried conductor pattern having a plate-shaped pattern.

Claims 49-50 (Cancelled).

51. (Currently amended) The integrated circuit of claim ~~50~~ 46, wherein said ~~conductive~~ at least one buried conductor pattern is formed of a material ~~is~~ selected from the group consisting of copper, copper alloy, silver, silver alloy, gold, gold alloy, tungsten, tungsten alloy, aluminum and aluminum alloy.

52. (Original) The integrated circuit of claim 46, wherein said monocrystalline substrate is a silicon substrate.

53. (Original) The integrated circuit of claim 46, wherein said monocrystalline substrate is a germanium substrate.

54. (Original) The integrated circuit of claim 46, wherein said monocrystalline substrate is a silicon-on-insulator substrate.

55. (Original) The integrated circuit of claim 46, wherein said monocrystalline substrate is a silicon-on-nothing substrate.

56. (Currently amended) A buried conductor pattern within a substrate, comprising:

at least one empty-spaced pattern in said substrate formed by annealing said substrate containing at least one hole drilled therein, said empty-spaced pattern having one of a sphere-shaped, plate-shaped, or pipe-shaped configuration; and

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a conductive material filling said empty space pattern such that at least a portion of a top surface of said conductive material is below a top surface of said substrate and at least a portion of a bottom surface of said conductive material is above a bottom surface of said substrate, said buried conductor pattern forming at least a part of an interconnect between devices.

Claim 57 (Cancelled).

58. (Original) The buried conductor pattern of claim 56, wherein said empty-spaced pattern has a pipe-shaped configuration.

59. (Original) The buried conductor pattern of claim 56, wherein said empty-spaced pattern has a plate-shaped configuration.

60. (Original) The buried conductor pattern of claim 56, wherein said empty-spaced pattern has a sphere-shaped configuration.

61. (Original) The buried conductor pattern of claim 56, wherein said substrate is a monocrystalline substrate.

62. (Currently amended) A processor system comprising:

a processor; and

a circuit coupled to said processor, at least one of said circuit and processor comprising:

a conductive structure comprising a substrate having at least one empty space pattern formed by annealing said substrate having at least one hole drilled therein, said empty-spaced pattern having one of a sphere-shaped, plate-shaped, or pipe-shaped configuration; and

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a conductive material filling said empty space pattern such that at least a portion of a top surface of said conductive material is below a top surface of said substrate and at least a portion of a bottom surface of said conductive material is above a bottom surface of said substrate, said conductive structure forming at least a part of an interconnect between devices.

63. (Currently amended) The processor based system of claim 62, wherein said empty-spaced pattern has a ~~configuration selected from the group consisting of~~ pipe-shaped configuration~~, sphere-shaped configuration and plate-shaped configuration~~.

64. (Original) The processor system of claim 62, wherein said empty-spaced pattern has a plate-shaped configuration.

65. (Original) The processor system of claim 62, wherein said empty-spaced pattern has a sphere-shaped configuration.

66. (Original) The processor system of claim 62, wherein said substrate is a monocrystalline substrate.

67. (Original) The processor system of claim 62, wherein said circuit is a memory circuit.

68. (Original) The processor system of claim 62, wherein said circuit is a DRAM memory circuit.

69. (Original) The processor system of claim 62, wherein said circuit and said processor are integrated on same circuit.

70. (Original) The processor system of claim 62, wherein said processor comprises said conductive structure.

71. (Original) The processor system of claim 62, wherein said circuit comprises said conductive structure.

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72. (Currently amended) An integrated circuit substrate comprising at least one buried conductor pattern provided within a monocrystalline substrate ~~and surrounded by semiconductor material~~ such that at least a portion of a top surface of said buried conductor pattern is below a top surface of said substrate and at least a portion of a bottom surface of said buried conductor pattern is above a bottom surface of said substrate, said at least one buried conductor pattern having a plate-shaped pattern and forming at least a part of an interconnect between devices, and a conductive path extending from said buried conductor pattern.

73. (Previously added) The integrated circuit of claim 72, further comprising a second buried conductor pattern having a pipe-shaped pattern.

74. (Previously added) The integrated circuit of claim 73, further comprising a third buried conductor pattern having a spherical pattern.

75. (Currently amended) An integrated circuit substrate comprising at least one buried conductor pattern provided within a monocrystalline substrate ~~and surrounded by semiconductor material~~ such that at least a portion of a top surface of said buried conductor pattern is below a top surface of said substrate and at least a portion of a bottom surface of said buried conductor pattern is above a bottom surface

of said substrate, said at least one buried conductor pattern having a pipe-shaped pattern and forming at least a part of an interconnect between devices, and a conductive path extending from said buried conductor pattern.

76. (Currently amended) An integrated circuit substrate comprising ~~at least two~~ first and second buried conductor patterns provided within a monocrystalline substrate ~~and surrounded by semiconductor material~~ such that at least a portion of a top surface of each of said buried conductor patterns is below a top surface of said substrate and at least a portion of a bottom surface of each of said buried conductor patterns is above a bottom surface of said substrate, said first and second buried conductive patterns forming at least a part of first and second interconnects between devices, respectively, wherein ~~a~~ said first ~~of said at least two~~ buried conductor ~~patterns~~ pattern is located below ~~a~~ said second ~~of said at least two~~ buried conductor ~~patterns~~ pattern and relative to ~~a~~ said surface of said monocrystalline substrate, and a first conductive path extending from said first ~~of said at least two~~ buried conductor ~~patterns~~ pattern and a second conductive path extending from said second ~~of said at least two~~ buried conductor ~~patterns~~ pattern.

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77. (Currently amended) The integrated circuit of claim 76, further comprising a third buried conductor pattern located below said ~~at least two~~ first and second buried conductor patterns and relative to a surface of said monocrystalline substrate and a third conductive path extending from said third buried conductor pattern.

78. (Currently amended) The integrated circuit of claim 77, wherein ~~said at least~~ one of said buried conductor patterns has a pipe-shaped pattern.

79. (Currently amended) The integrated circuit of claim 77, wherein ~~said at least~~ one of said buried conductor patterns has a plate-shaped pattern.

80. (Currently amended) The integrated circuit of claim 77, wherein ~~said at least~~ one of said buried conductor patterns has a spherical pattern.

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81. (Currently amended) The integrated circuit of claim 77, wherein said ~~conductive~~ buried conductor patterns are formed of a conductive material selected from the group consisting of copper, copper alloy, silver, silver alloy, gold, gold alloy, tungsten, tungsten alloy, aluminum and aluminum alloy.